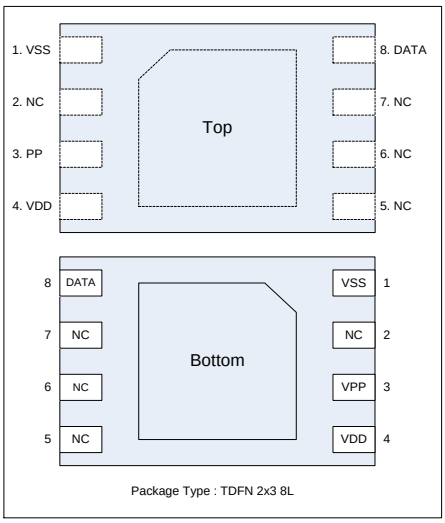
Features

- Cipher Algorithm : Applied AES-128
- Digital Controlled OTP Memory (32Bytes)
- 1.65 ~ 4.8V Operation Voltage
- Built-in POR
- Built-in OSC
- 8 Bytes OTP ROM cell for User Serial
- Two Power Mode(Active, Standby)
- Adjustable Standby Enable Time
- Communication : ART(1) interface (up to 20 kbps)

Applications

- DMB, Navigation
- Mobile Phone, PMP, MP3
- DVR(PVR), DVDP, STB
- Battery
- Etc.(Most of electronic system using u-Processor)

Pin Configuration



General Description

The ALPU-P is strong encryption chip even in turbulent circumstance such as static electricity. Valuable products made with strong encryption can be prevented competitor from being copied with the least expense or efforts and an amount of production can be tracked with a unique serial number in individual chip.

Typical Application

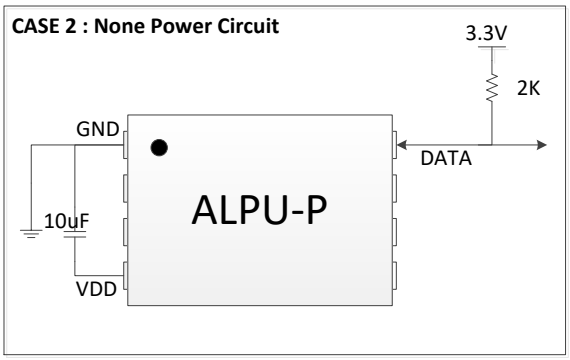


Figure 1. Typical application with the ALPU-P

Encryption Flow

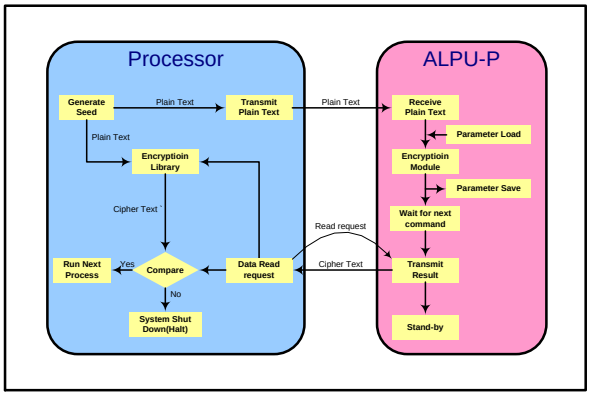


Figure 2. Operation Diagram

Note (1) ART : Adaptive Reference Time

Contents

1 Overview

The illegal copy products being sold, enterprises have suffered economic injury and the reliability of the product lose public confidence. And also lose one's dignity. ALPU is authentication chip to keep away like this illegal copy. As specialized in the electrical component, the fact that electric current consuming is few is feature. And in order serviceable even in the battery pack, it supports ART(1) 1-Line communication. The ALPU-P is having two kinds of power mode, Standby-Mode and Active-Mode. In case which will be a Standby-Mode, there is not electric current consuming almost and it is suitable to apply with handhelds.

1.1 Feature

Advance chip to prevent illegal copy

The 128 bits encryption which applied the AES-128

Reference Operating Voltage : 1.65 ~ 4.8V

Communication : ART 1-Line Interface (up to 20 kbps)

8 Bytes OTP ROM cell for User Serial

Two Power Mode (Active and Standby)

Built-in POR(Power on Reset

Built-in OSC(1 MHz Oscillator)

Package : TDFN-8L 2mm x 3mm

1.2 Block Diagram

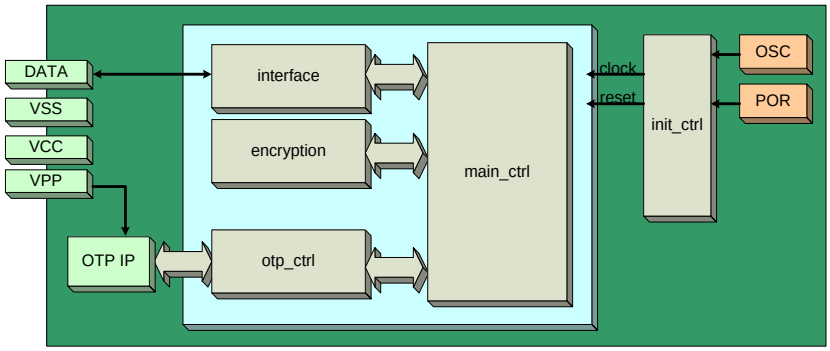


Figure 1-1. Block Diagram

ALPU-P is composed of a digital block and a analog block. Analog block consists of OTP, OSC and POR, Digital block consists of interface, encryption, otp_ctrl and main_ctrl, It does control the OTP, encryption communication and so on through main_ctrl block.

1.3 PIN Configuration

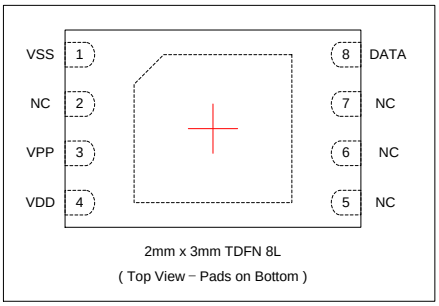


Figure 1-2. 2mm x 3mm TDFN 8L Pin Configuration(refer to chapter 12.1 POD-TDFN-8L)

1.4 PIN Description

Table 1-1. Package type TDFN-8L 2x3

PIN No.	Pin Name	Description
1	VSS	Ground
2	NC	None Connect
3	VPP	Write : 6.5V Supply for programming OTP cells Read : VPP same as VDD for Read
4	VDD	Charge Capacitor
5	NC	None Connect
6	NC	None Connect
7	NC	None Connect
8	DATA(1)	Communication Line

2 PORT

ALPU-P has different I/O types as shown in table 2-1.

Table 2-1. I/O Type

Name	Direction	Description
VSS	PWR	Ground
VDD	PWR	Charge Capacitor
DATA	Bi-direction	CMOS input / Open-Drain Output

3 Clock Management

3.1 Internal clock

Parameter Internal oscillator is used from all digital blocks. Frequency is 1MHz shown in Table 3-1.

Table 3-1. Internal OSC parameter (Ta = 25℃)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Frequency	f_{OSC}		-	1	-	MHz
Frequency variation	Δf_{OSC}		-	-	10	%
Duty cycle	D		-	50	-	%

3.1.1 Oscillator On/Off

Internal oscillator can be turned on and off. If ALPU-P is in the condition of Standby-Mode, then internal oscillator is not operate, it is turned off low-power.(refer to chapter 4. Power Mode)

4 Power Mode

ALPU-P supports two types of the poser mode. In case of Standby-Mode, internal oscillator do not work so that electric current consuming decreases. To make the Standby-Mode, keep the DATA pin high or low more than 2 seconds. To make Active-Mode, cross the DATA pin from high to low or from low to thing, then it will wake-up.

4.1 Standby-Mode Condition

Here is the condition to enter the Standby-Mode. DATA pin is keeping high and low more than t_{SMOT}. (refer to Table 4-1)

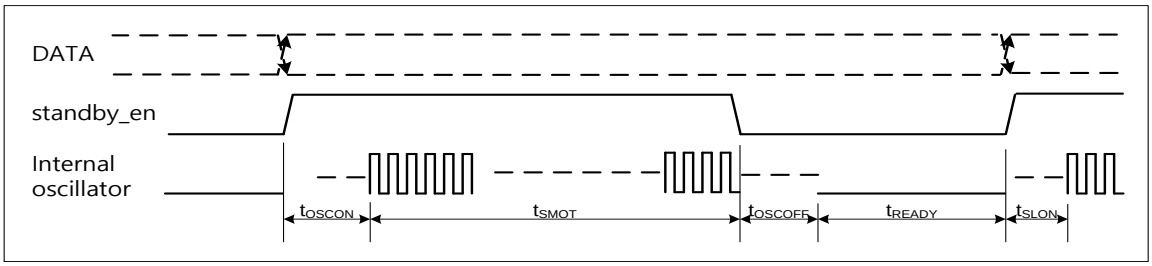


Figure 4-1. Standby-Mode Waveform

DATA : Serial Data

standby_en : Internal OSC Standby Enable Signal

Internal Oscillator : 1MHz Oscillator for internal logic

Table 4-1. Standby-Mode Waveform Parameters (The basic frequency 1MHz)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Standby-Mode on Time	$t_{SMOT(2)}$	128		1024-	Ms
Ready	t_{READY}	t_{READY} period is finished when the DATA is transited			
OSC on Time	t_{OSCON}	10	50	-	us
OSC Off Time	t_{OSCOFF}			1	us

Note : (2) refer to chapter 4.3 standby-Mode on time set

4.2 Active-Mode

Ina Standby-Mode, cross the DATA pin from high to low or from low to high, then it will wake-up.

4.3 Standby-Mode on time set

Initially t_{SMOT} is set at 128ms. But t_{SMOT} can be modified only once by customer's requirement such as one of Table 4-2 the Standby-Mode. Contact with NEOWINE if customer want to change other type on the Table 4-2 the Standby-Mode on time.

Table 4-2 Standby-Mode on Time

Standby-Mode on time select	Standby-Mode on time		
	MIN	TYP	MAX
0	-	1,024	-
1	-	512	-
2	-	256	-
3	-	128	-

Unit : ms

5 Initialization

ALPU-P has an internal POR circuit, POR is not necessary extern reset separately.(refer to Figure 5-1_

5.1 Start-up Waveform

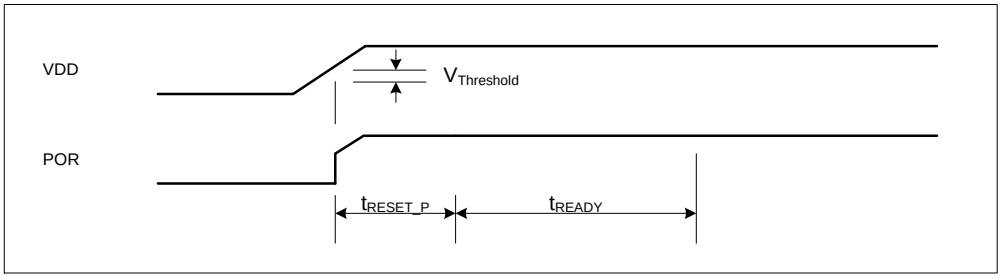


Figure 5-1. Start-up Waveform

VDD : Supplied power

POR : Internal Power On Reset Signal

register : Internal registers for initialization

Table 5-1. Start-up Timing Parameters.

Parameter	Symbol	Min	Typ	Max	Unit
Threshold Voltage	$V_{Threshold}$	1.26			V
POR Reset Time	t_{RESET_P}	30			us
Chip Ready	t_{READY}	t_{READY} period is finished when the DATA is transited.			
Initial Time	$t_{INITIAL}$	250			us

5.2 Internal Power On Reset

A POR pulse is generated by on chip detection circuit. The detection level is defined in Table 5-1. The POR is activated whenever DATA is lower than the detection level($V_{Threshold}$). Reaching the POR $V_{Threshold}$ invoke the delay counter, which has the some reset time(t_{RESET_P}). t_{RESET_P} period is finished when the DATA is transited.

6 Encryption

6.1 Encryption Core Block Diagram

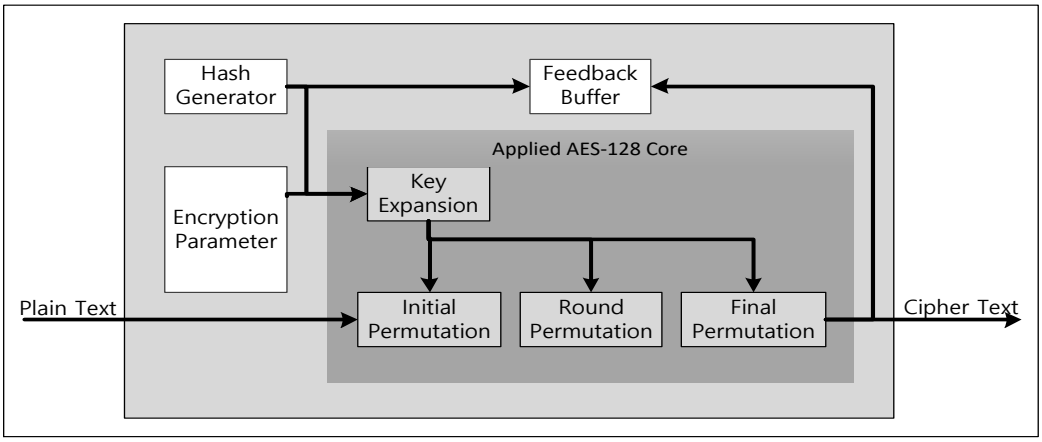


Figure 6-1. Encryption Core Block Diagram

ALPU-P is 128 bits encryption core applied with AES128. The core consists of several block which are AES128 core, Random Counter, Feedback Buffers and Encryption Parameter.

6.2 Encryption Configured with sub-address

Encryption core is configured with sub-address as shown in figure 6-1.

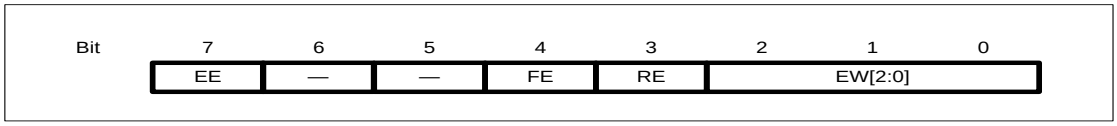


Figure 6-2. Sub-Address Configuration

bit 7 : EE (Encryption Enable)

When EE bit is set ‘1’, it is in encryption mode.

bit 6 : Fixed ‘0’

bit 5 : fixed ‘1’

bit 4 : (Feedback Enable)

When both EE and FE bit are set to ‘1’, it is in feedback mode

bit 3 : RE(Hash Enable)

When both EE and RE bit are set to ‘1’, it is pseudo Hash Counter.

bit 2~0 : EW (Encryption Width)

The EW bits are loop count numbers of the encryption algorithm.

6.3 Encryption Mode

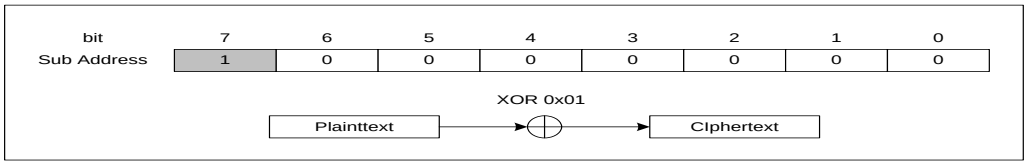


Figure 6-3. Bypass mode sub-address Construction

6.3.1 Bypass Encryption Mode

Bypass is a mode to test the communication interface between MCU and ALPU-P. The data(Xn) from MCU will do Exclusive-OR operation with 0x01 in ALPU-P.

6.3.2 Feedback Encryption

It is not able to open this information

6.3.3 Hash Counter Mode

It is not able to open this information

6.4 Encryption Flow

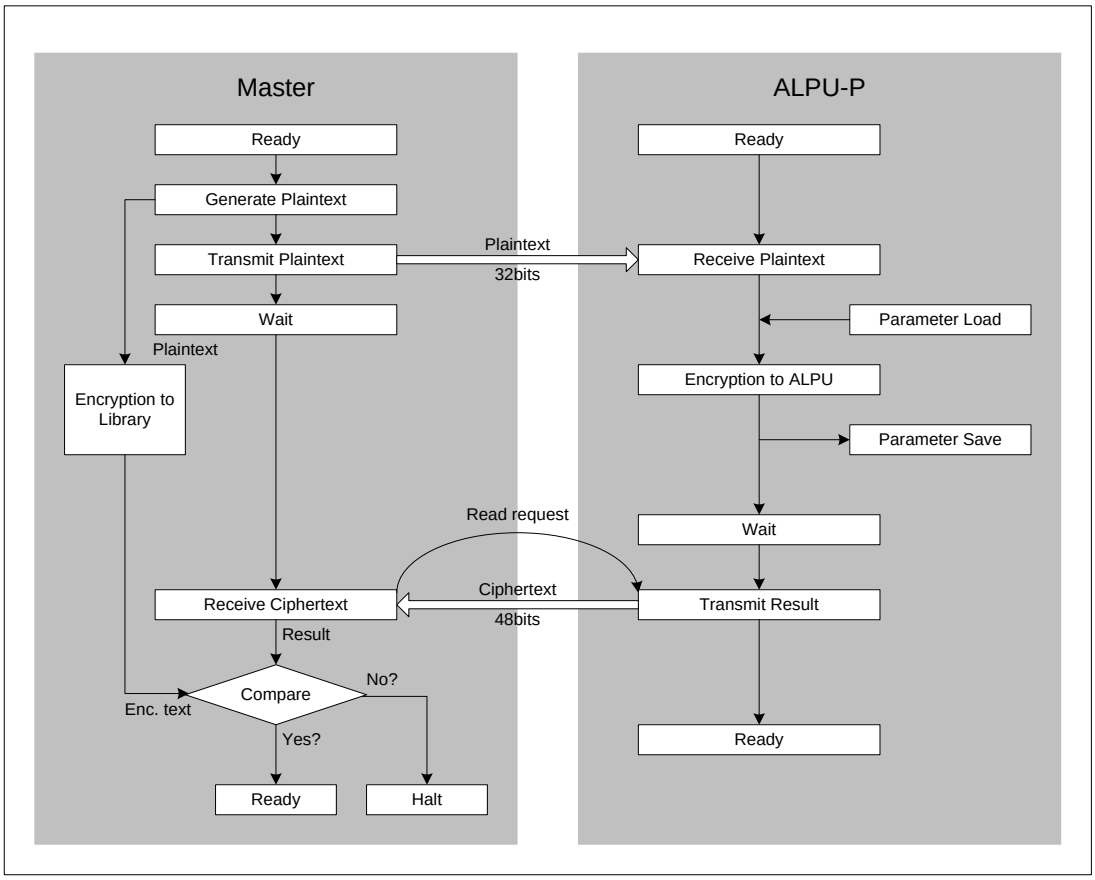


Figure 6-4. Encryption Flow

7 Communication Packet Structure

7.1 Write Packet Structure

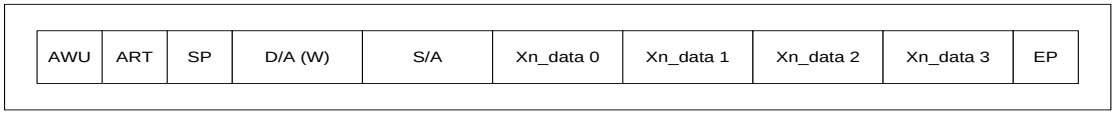


Figure 7-1. Write packet structure

AWU : ART Wake-up

ART : Adaptive Reference Time

SP : Start Preamble

EP : End Preamble

D/A(W) : Device Address(Write)

S/A : Sub-Address

Xn_data0~3 : 4 Bytes Write Data(Plain-Text)

7.2 Read Packet Structure

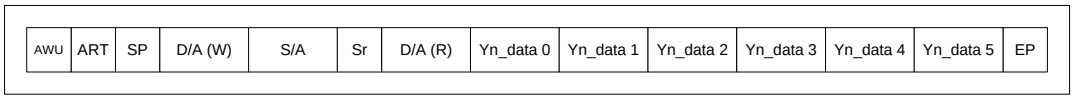


Figure 7-2. Read packet structure

AWU : ART Wake-up

ART : Adaptive Reference Time

SP : Start Preamble

EP : End Preamble

D/A(W) : Device Address(Write)

D/A(R) : Device Address(Read)

S/A : Sub-Address

Yn_data0~5 : 6 Bytes Read Data(Cipher-Text)

7.3 Implementation

7.3.1 Bypass Mode

```
// Bypass Mode Set
sub_address = 0x80;

// Plaintext Generate
for ( i=0; i<4; i++) alpup_tx_data[i] = _alpu_rand();

// Write Plaintext Data to ALPU-P
_art_write(device_address, sub_address, alpup_tx_data, 4);

// Read Data from ALPU-P
_art_read(device_address, sub_address, alpup_rx_data, 6);

// Bypass Encryption  ( XOR operation )
for ( i=0; i<4; i++) alpup_ex_data[i] = alpup_tx_data[i] ^ 0x01;

// Compare the encoded data and received data
for (i=0; i<4; i++) {
        if (alpup_rx_data[i] != alpup_ex_data[i]) return 1; // Fail
}
return 0: // Pass
```

Figure 7-3. Bypass Mode example C code

1. Generated plain-text with the hash data
2. Write plain-text to ALPU-P
3. Read cipher-text from ALPU-P
4. Compare the encrypted data and received data

8 OTP (One Time Programmable) ROM

ALPU-P has 256 bits OTP memory. It can be programmed through ART 1-Line Interface. User give the DC power 6.5V to ALPU-P's OTP pin during the OTP write. User can write 64 bits OTP area except 192 bits OTP area.

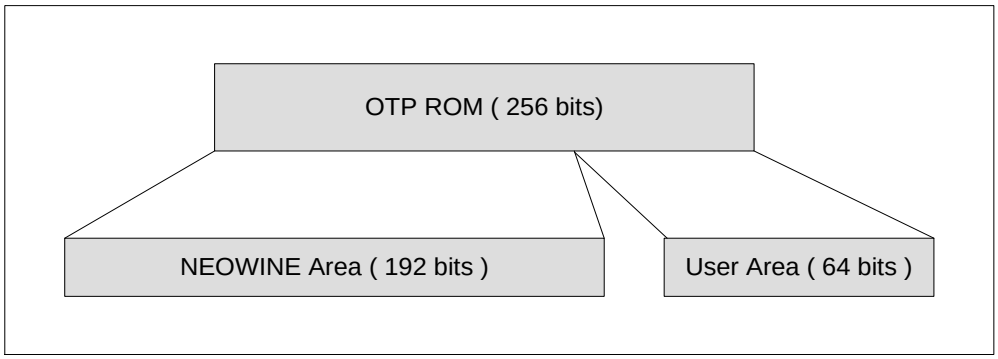


Figure 8-1. OTP Memory Map

8.1 Definition of timing(OTP Read of User Area)

Figure 8-2 shows the OTP access signal reading data from ALPU-P. The t_{OTP_READ} time is necessary in accessing data.

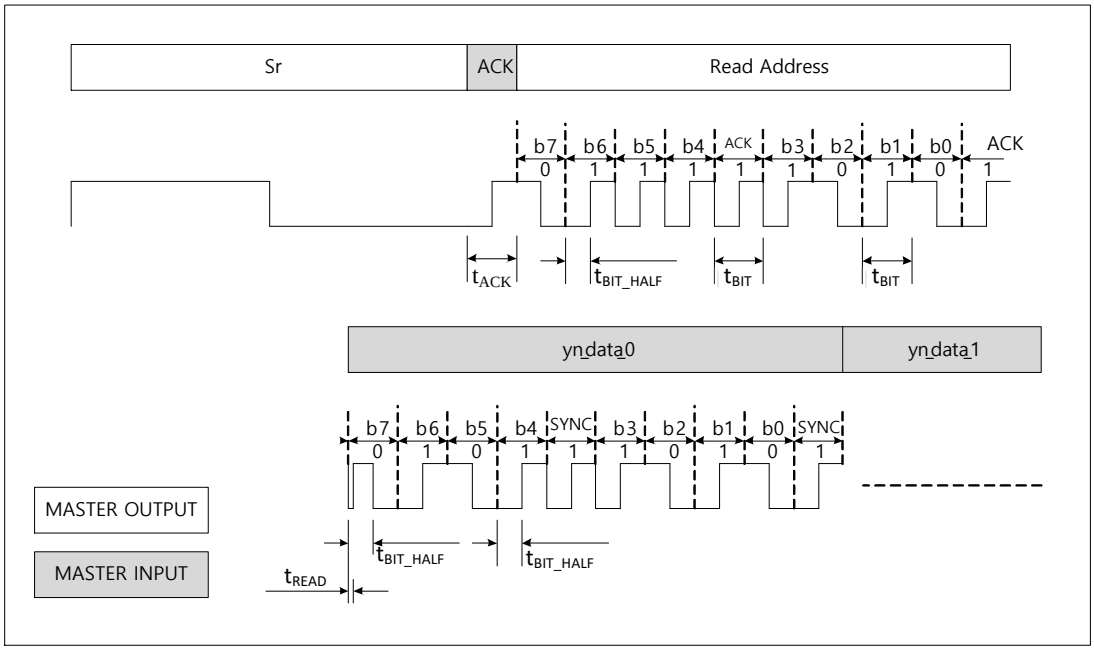


Figure 8-2. OTP Access Signal

Table 8-1. OTP Access Timing

Parameter	Symbol	Communication Speed			Unit
		Min	Typ	Max	
ART One Bit Time	t_{BIT}	200	100	50	us
Half to Bit Time	t_{BIT_HALF}	100	50	25	us
OTP Access Time	t_{OTP_READ}		10		us

9 Communication Interface

9.1 ART 1-Line Interface

ART 1-Line communication is suitable to be applied in MCU. It operates as slave, and can be

available 128 different device with just one MCU GPIO pin when ART protocol applied. 128 device must have different device address each other, and pull-up resistor is required on the data line. ART 1-Line interface is the format which NEOWINE is originative, and it is possible to support the speed from 5kbps to 20kbps.

9.1.1 Write packet structure

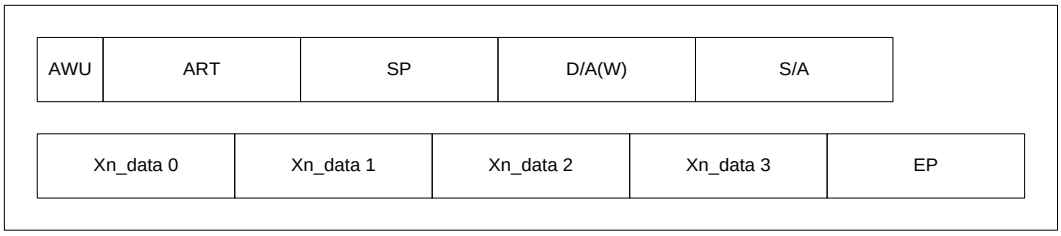


Figure 9-1. Write packet structure

AWU : ART wake-up

ART : Adaptive Reference Time

SP : Start Preamble

D/A(W) : Device Address(Write)

S/A : Sub-Address

Xn_data 0~3 : Write Data(Plain-text)

EP : End Preamble

9.1.2 Read packet structure

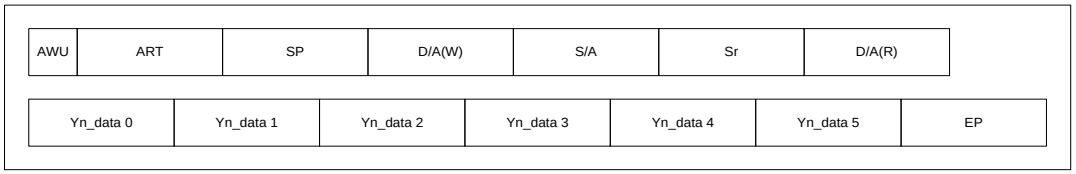


Figure 9-2. Read packet structure

AWU : ART wake-up

ART : Adaptive Reference Time

SP : Start Preamble

D/A(W) : Device Address(Write)

Sr : Repeated Start

D/A(R) : Device Address(Read)

S/A : Sub-Address

Xn_data 0~3 : Write Data(Plain-text)

EP : End Preamble

9.1.3 Start Preamble Structure

Figure 9-3 shows the START PREAMBLE structure of ALPU-P. ALPU-P transmits true(1) value for acknowledge, if the ALPU-P receive a correct START PREAMBLE.

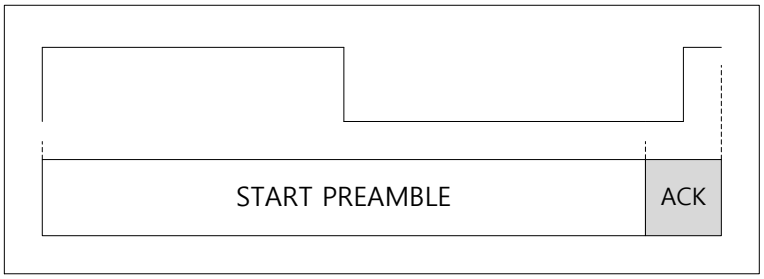


Figure 9-3. Start Preamble Structure

9.1.4 Byte Structure

Figure 9-4 shows the byte structure of write data. ALPU-P transmits true(1) value every 4 bits for acknowledge.

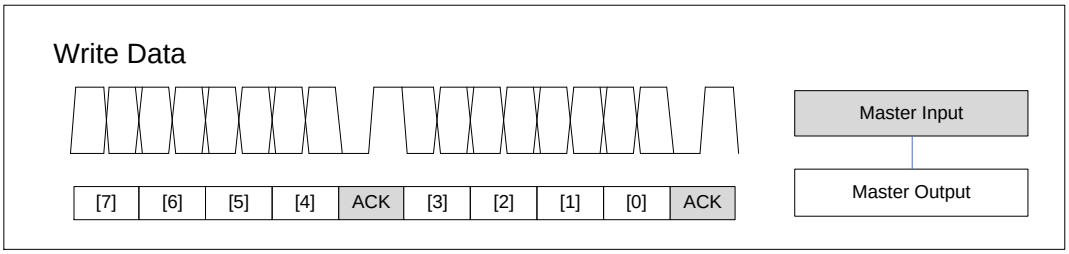


Figure 9-4. Write Byte Structure

Figure 9-5 shown the byte structure of read data. MCU should transmit sync signal, High, to ALPU-P after receiving 4 bits data from ALPU-P.

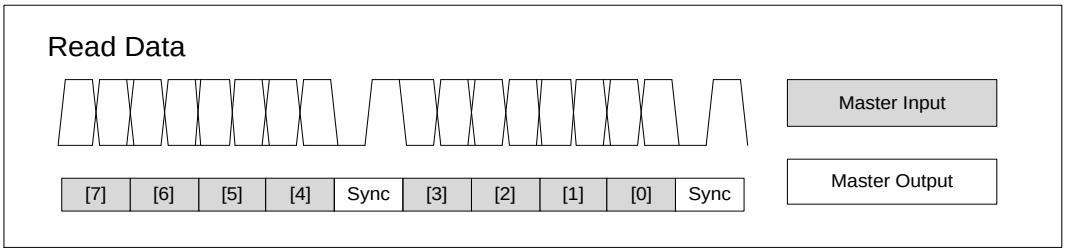


Figure 9-5. Read byte packet

9.1.5 Waveform

Figure 9-6 shown the Write/Read waveform.

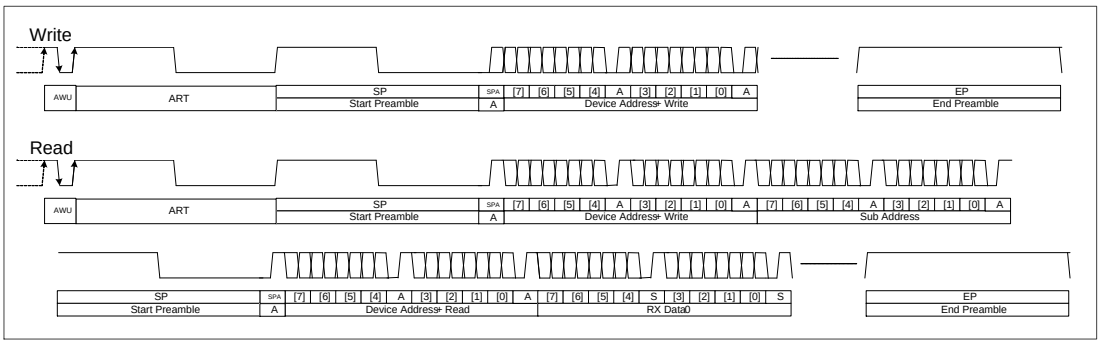


Figure 9-6. ART 1-Line Waveform

9.1.6 Definition of Timing

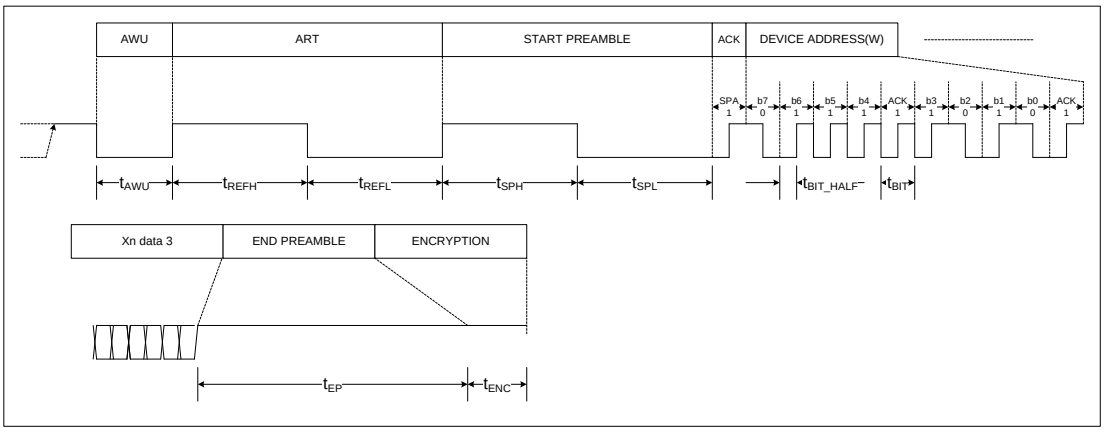


Figure 9-7. Definition of Timing

Table 9-1. ART Timing Parameters.

Parameter	Symbol	Rate	Communication Speed			Unit
			Min	Typ	Max	
Communication Speed		-	5	10	20	kbps
ART Wake Up Time	t_{AWU}	-	30	50	100	us
Adaptive Reference High Time	t_{REFH}	t	800	400	200	us

Adaptive Reference Low Time	t_{REFL}	t	800	400	200	us
Start Preamble High Time(Start)	t_{SPH}	t	800	400	200	us
Start Preamble Low Time(Start)	t_{SPL}	t	800	400	200	us
Start Preamble Ack	t_{SPA}	t/4	200	100	50	us
ART One Bit Time	t_{BIT}	t/4	200	100	50	us
Half to Bit Time	t_{CODE}	t/8	100	50	25	us
End Preamble (Stop)	t_{EP}	2t	1600	800	400	us
Encryption Time	t_{ENC}	-		1000		us

10 Electrical Characteristic

10.1 Absolute Maximum Rating (Reference to VSS)

Supply Voltage : 5.5V

All other pins : -0.5V to DATA + 0.5V

ESD Rating

HBM(1) : 2000V

MM(2) : 200V

CDM(3) : 800V

Note : (1) HBM(Human Body Model), (2) MM(Machine Model), (3) CDM(Changed Device Model)

10.2 Recommended Operating Condition

Ambient temperature rand : TBD

10.3 DC Characteristic

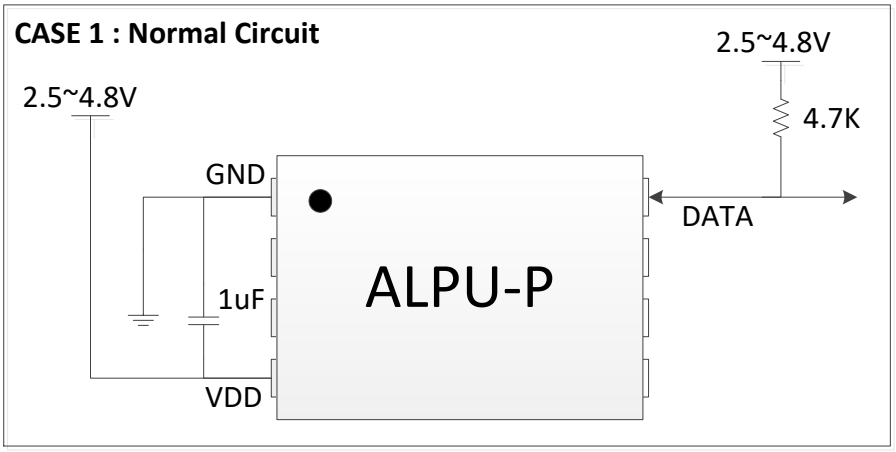
Table 10-1. DC Characteristic

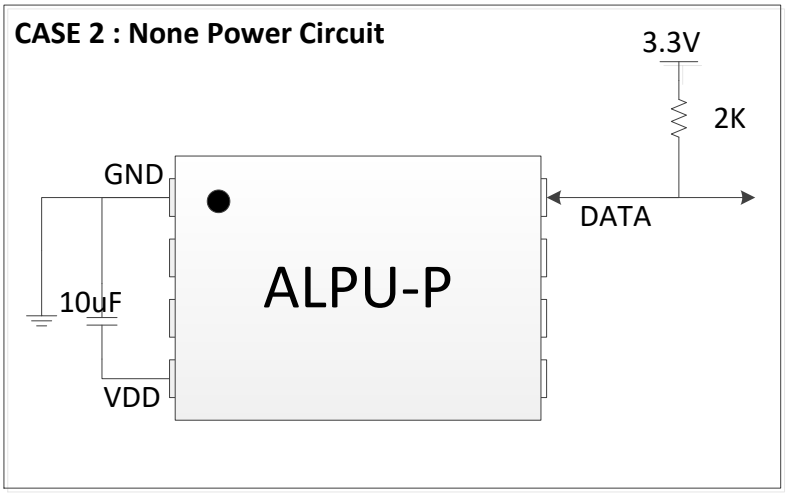
Parameter	Symbol	Condition	Min	Typ	Max	Unit

DC Characteristics						
Supply Voltage	V_{DD}	During normal operation	3.0	3.3	3.6	V
Active-Mode supply current (exclude I/O current)	I_{DD}	DATA=3.3V		250		uA
Standby mode supply current	I_{DDS}	DATA pin stay high or low more than Standby on time			1	uA
OTP programming mode supply current	I_{DDP}	For ~ 1ms duration per write operation	-	-	256	uA
Internal OTP programming voltage	V_{PP}	Observable only in OTP write	6.25	6.5	6.75	V
POR Release Threshold	V_{POR+}		1.32			V
POR Assertion Threshold	V_{POR-}		1.26			V
DATA Pin Characteristics						
DATA Input Low Voltage	V_{IL}		-0.4		0.5	V
DATA Input High Voltage	V_{IH}		1.5		V_{DD} +0.4	V
DATA Internal Pull-up Current	I_{PU}	DATA = 3.3V			1	uA
DATA Output Low Voltage	V_{OL}	I_{OL} = mA			0.4	V
DATA Output Fall Time	t_F	90% to 10%, C_{LOAD} = 12pF			5	ns
DATA Capacitance	C_{PIN}			6		pF

11 Typical Operation Circuit

11.1 ALPU-P Operation Circuit





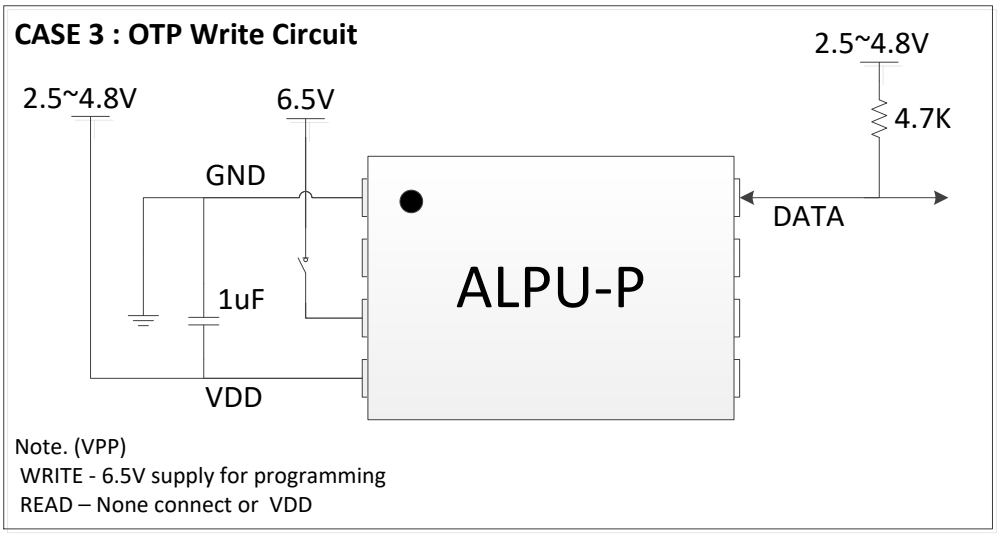
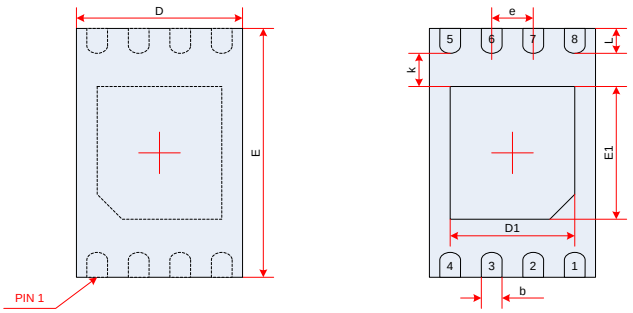


Figure 11-1. Operation Circuit

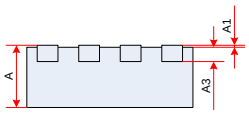
12 Package Information

12.1 POD-TDFN-8L 2mm x 3mm

DFNWB2X3-8L (P0.50T0.55/ 0.60) PACKAGE OUTLINE DIMENSIONS



Top View **Bottom View**



Side View

SYMBOL	Dimension In Millimeters		Dimension In Inches	
	Min.	Max.	Min.	Max.
A	0.450/0.500/0.550	0.550/0.600/0.650	0.018/0.020/0.022	0.022/0.024/0.026
A1	0.000	0.050	0.000	0.002
A3	0.152REF.		0.006REF.	
D	1.924	2.076	0.076	0.082
E	2.924	3.076	0.115	0.121
D1	1.400	1.600	0.055	0.063
E1	1.300	1.500	0.051	0.059
K	0.200MIN.		0.008MIN.	
b	0.20	0.30	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.224	0.376	0.009	0.015

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